**Remarks/Arguments**

In the application claims 1-17 are pending and Examiner has rejected claims 9 and 11-17. Claims 1-8 are allowed. In this response, no claims are amended.

**35 U.S.C. §102**

Examiner has rejected claims 9 and 14 as being anticipated by cited reference 1 (US 5,502,502A). Applicant respectfully disagrees that the reference anticipates claim 9. Claim 9 recites, inter alia, "examining a sync signal for the presence of one or more sync pulses; outputting those said one or more svnc pulses as drive pulses if said sync pulses are present" (emphasis added). This is a clear statement that the method of claim 9 comprises outputting the one or more sync pulses when the sync pulses are present in the sync signal. In contrast, the cited reference teaches to output drive pulses that are developed by a phase locked loop, not the actual input sync pulses.

Please refer to reference 1 in column 4, lines 21-23, "what is important is that while H sync is present, H drive is generated by counts that are controlled by H sync through gated H sync and PLL 16." Kindly also see column 4, line 66 - column 5, line 1 "the horizontal counter logic 14 thus counts pulses from PLL 16 and generates an H Drive signal at a predetermined count". It is clear that the technical solutions are not the same.

Please now look to the English language version of the present application on page 1, line 18 - page 2, line 5. "In the past this function of generating the horizontal time base signal has been done using either a phase locked loop or a synchronized oscillator. Each of these approaches can satisfy the objectives of providing a synchronized horizontal drive signal when a video input is received and a free-running horizontal time base signal otherwise; however, each has significant negative attributes. The phase locked loop suffers due to its cost and complexity as well as its potential phase jitter. Synchronized oscillators, usually either blocking oscillators or synchronized astable multivibrators, both suffer from the problem that when they are synchronized to horizontal sync, the output

horizontal time base signal pulse width is determined by the oscillator components rather than the incoming horizontal sync. Due to this characteristic, events relying on the horizontal drive pulse width may vary as a function of temperature and component aging. A further problem with both the phase locked loop and synchronized oscillator approaches is that the output horizontal time base signal does not contain the equalizing pulses of the received horizontal sync signal. The present invention provides a circuit and a method for providing a horizontal time base signal that approximates horizontal drive when no video signal is present and when horizontal sync is absent during the vertical interval of a received video signal. This invention also provides a pass-through of the incoming horizontal sync during the times when said horizontal sync is present, thus eliminating timing and pulse width uncertainties." Also, please note page 5, lines 16-24. "Looking now to the timing diagram figure 4, if signal S12, is present and contains a logic 0 pulse during time Ts, and the pulse width of monostable 110, $T_{140}$, is shorter than the width of the horizontal sync pulse, Ts, both the leading and trailing edges of signals S14 and S20 will be coincident with the leading and trailing edges of the input horizontal signal S12. As a consequence of signal S12 being held in a logic 0 state longer than the pulse duration $T_{140}$, horizontal drive signal S20 "follows" signal S12 (albeit in an inverted form) with only a minimal propagation delay. Typical propagation delays for the monostables used in the preferred embodiment are approximately 20 nSeconds. Even delays much greater than this would be substantially coincident if they are reasonably predictable", and page 7, lines 14-18 "figure 9 is a flow diagram of an embodiment of the invention. The method comprises the steps of examining, in decision block 310 an input sync signal S10 to determine if sync pulses are present and either transmitting the input sync pulses directly to the output drive signal in action block 320 or enabling a free running oscillator to output drive signals in action block 330." In view of these observations, it is also clear that the reference can not achieve the same technical effect as the present application.

Regarding Examiner's rejection of independent claim 14, as discussed above with reference to claim 9, reference 1 is a PLL based system and does not disclose "means for transmitting sync pulses from said input sync signal to said drive signal when said sync pulses are present" as recited in claim 14. Since

reference 1 does not disclose each and every element of claim 14, it does not anticipate claim 14. Applicant respectfully requests that the Examiner withdraw the rejection of claims 1 and 9.

Examiner has rejected dependent claims 11-13 and 15-17 as being disclosed by reference 1. Claims 11-13 and 15-17, being dependent on an allowable base claim or claims depending from an allowable base claim, are themselves allowable. Withdrawal of the rejection of claims 11-13 and 15-17 is respectfully requested.

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (317) 587-4029, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,

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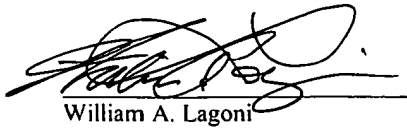

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